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Estimation of Leakage Power using Power Reduction Circuit

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***Abstract* - Scaling Associate in Nursingd power reduction trends in future technologies can cause subthreshold run currents to become an progressively massive part of total power dissipation. the big run power consumption is especially hard in mobile devices, wherever the battery charge capability poses a demanding limitation on the entire energy which will be consumed by a chip. during this technique, sleep transistor square measure placed between the circuits offer and provide rails to show off the run current flow throughout idle time this will be done by victimization one PMOS transistor and one NMOS transistor nonparallel with the transistors of every logic block to make a virtual ground and a virtual power supply. constant estimation victimization town simulation will acquire a comparatively correct estimation of the run distribution; but, this methodology needs an extended simulation time and is therefore computationally expensive. The static and dynamic power of a sleep stack is significantly low. however it's a delay penalty and its space demand is most compared with different processes. once the a sleep keeper method possesses wonderful speed criteria however it needs more static and dynamic power than a sleep stack. Our goal is to trade off between these limitations and therefore propose new ways that scale back each run and dynamic power with minimum attainable space and delay trade off.**

***Keywords* – Leakage Power, Power Reduction Circuit, PMOS Transistor, NMOS Transistor**

I. Introduction

Power and reliableness became 2 key style goals with technology reducing. the most objective of this thesis is to supply new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, that is showing associate degree ever-increasing growth with the reducing of the technologies. numerous techniques at the various levels of the planning method are enforced to cut back the power dissipation at the circuit, study and system level. moreover, the quantity of gates per chip space is consistently increasing, whereas the gate change energy doesn't decrease at identical rate, that the power dissipation rises and warmth removal becomes harder and big-ticket. Then, to limit the power dissipation, different solutions at every level of abstraction square measure projected. As technology scales, negative bias temperature in stability (NBTI) is rising united of the foremost reliableness degradation mechanisms. NBTI happens once PMOS transistors square measure negatively biased (Vgs= -Vdd) at elevated temperature, inflicting a shift within the threshold voltages. Over a protracted amount of your time, such shifts will doubtless cause a major increase within the delay of PMOS devices , and end in regarding 10%–20% degradation within the circuit speed, doubtless resulting in a practical failure. Consequently, it's vital to model, analyze, and mitigate the impact of the NBTI result on the circuit performance. As technology scales, the aging result caused by negative bias temperature instability (NBTI) has become a significant reliableness concern. within the mean solar time, reducing outflow power remains to be one among the key style goals. as a result of each NBTI-in- duced circuit degradation and standby outflow power have a powerful dependency on the input vectors, input vector management (IVC) technique may be adopted to cut back the outflow power and mitigate NBTI-induced degradation.

II. Releated Work

CMOS technology scaling enhances the computing capability of integrated circuits. Increasing numbers of miniaturized transistors are crammed onto integrated circuits, thereby enhancing the functionality. In paper publish by Yu Wang, Xiaoming Chen, Wenping Wang, Yu Cao, Yuan Xie, and Huazhong Yang "Leakage Power and Circuit Aging Cooptimization by Gate Replacement Techniques" in IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 4, April 2011. In their paper they propose 2 gate replacement algorithmic programs [direct gate replacement (DGR) algorithm and divide and conquer-based gate replacement (DCBGR) algorithm], along side optimal input vector choice, to at the same time reduce the leakage power and mitigate NBTI-induced degradation. They use the input vector management technique by sleep transistor technique to research the leakage power in MOSFET. They left the future work as there's a provision to scale back the leakage power additional exploitation logic synthesis combined with the gate replacement technique which can result in higher co optimisation results.

Hailong Jiao,and Volkan Kursun publish their paper on title "Reactivation Noise Suppression With Sleep Signal Slew Rate Modulation in MTCMOS Circuits" in IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 21, No. 3, March 2013 pp no 533. . In their work they projected triple-phase sleep signal slew rate modulation technique enhances the tolerance to method

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parameter fluctuations by up to 183.1× as compared to numerous various MTCMOS noise suppression techniques in an exceedingly UMC 80-nm CMOS technology

Rakesh Gnana David Jeyasingh, Navakanta Bhat, and Bharadwaj Amrutur publish their paper on title "Adaptive Keeper Design for Dynamic Logic Circuits Using Rate Sensing Technique" in IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 19, No. 2, February 2011 pp no.295. In their work they style the circuit operation of RSK employing a thirty two eight register file enforced in Associate in Nursing industrial one30-nm 1.2-V CMOS method. The performance of individual dynamic logic gates also are evaluated on chip for numerous keeper techniques. we tend to show that the RSK technique provides superior performance compared to the opposite alternatives like Conditional Keeper (CKP) and current mirror-based keeper (LCR). They use a keeper junction transistor technique base current mirror circuit to cut back the delay at output node.

Our work is titled new low power approaches for VLSI logic and memory. whereas coming up with a VLSI system power dissipation is one among the foremost considerations. Up to a definite time dynamic power was the one largest concern; but because the technology feature size shrinks static power has become a very important issue as dynamic power.

III. Proposed Methodology

With the fast progress in semiconductor technology, chip density and operation frequency have inflated, creating the ability consumption in battery-operated moveable devices a serious concern. High power consumption reduces the battery service life. The goal of low-power style for powered devices is therefore to increase the battery service life whereas meeting performance necessities. Reducing power dissipation could be a style goal even for non-portable devices since excessive power dissipation ends up in inflated packaging and cooling prices yet as potential dependableness issues.

IC power dissipation consists of various parts depending on the circuit operative mode. First, the change or dynamic power part dominates during the active mode of operation. Second, there are 2 primary leakage sources, the active part and the standby leakage part. The standby leakage is also created considerably smaller than the active leakage by changing the body bias conditions or by power-gating.

Voltage scaling is maybe the foremost effective methodology of saving power due to the square law dependency of digital circuit active power on the availability voltage. unfortunately, scaling V_{DD} additionally reduces the circuit speed since the gate drive, $V_{GS} - V_T$, is reduced.

A. Sources Of Leakage Power

There are four main sources of leakage current in a CMOS transistor :

1. Reverse-biased junction leakage current (I_{REV})
2. Gate induced drain leakage (I_{GIDL})
3. Gate direct-tunneling leakage (I_G)
4. Subthreshold (weak inversion) leakage (I_{SUB})

1. Reverse-biased junction leakage current (I_{REV})

The junction leakage happens from the source or drain to the substrate through the reverse biased diodes once a junction transistor is OFF. A reverse-biased pn junction leakage has 2 main components: one is because of electron-hole pair generation within the depletion region of the reverse-biased junction; the other minority carrier diffusion/drift close to the edge of the depletion region.

2. Gate induced drain leakage (I_{GIDL})

The gate induced drain leakage (GIDL) is caused by high field impact within the drain junction of MOS transistors. For Associate in Nursing NMOS transistor with grounded gate and drain potential at V_{DD}, vital band bending significant drain permits electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is formed since the holes area unit apace swept intent on the substrate. At constant time, electrons are collected by the drain, resulting in GIDL current. This leakage mechanism is formed worse by high drain to body voltage and high drain to gate voltage. semiconductor device scaling has semiconductor diode to progressively steep halo implants, wherever the substrate doping at the junction interfaces is increased, whereas the channel doping is low.

3. Gate Direct Tunneling Leakage

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3–4 nm, this type of current results from the Fowler- Nordheim tunneling of electrons into the conductivity band of the oxide layer underneath a high applied field across the oxide layer. For lower oxide thicknesses (which are generally found in zero.15μm and lower technology nodes), however, direct tunneling through the silicon dioxide layer is that the leading impact. Mechanisms for direct tunneling embody electron tunneling within the conductivity band (ECB), electron tunneling within the valence band (EVB), and hole tunneling within the valence band (HVB), among that ECB is that the dominant one.The magnitude of the gate direct tunneling current will increase exponentially with the gate oxide thickness Tox and provide voltage V_{DD}. In fact, for comparatively thin oxide thicknesses (in the order of 2-3 nm), at a V_{GS} of 1V, every 0.2nm reduction in Tox causes a denary increase in IG. Gate leakage will increase with temperature at solely regarding 2x/100 . Note that the gate leakage for a PMOS device is often one order of magnitude smaller than that of associate NMOS device with identical Tox and V_DD once victimization SiO_2 because the gate nonconductor.

4. Subthreshold Leakage

The subthreshold leakage is that the drain-source current of a transistor operative within the weak inversion region. in contrast to the strong inversion region during which the drift current dominates, the subthreshold physical phenomenon is because of the diffusion current of the minority carriers within the channel for a MOS device. as an example, within the case of associate inverter with a low input voltage, the NMOS is turned OFF and therefore

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the output voltage is high. during this case, though V_{GS} is 0V, there's still a current flowing within the channel of the OFF NMOS transistor because of the V_{DD} potential of the V_{DS}. The magnitude of the subthreshold current may be a perform of the temperature, supply voltage, device size, and therefore the method parameters out of that the edge voltage (V_T) plays a dominant role.

In current CMOS technologies, the subthreshold leakage current, Isub, is way larger than the opposite leakage current parts. this can be chiefly as a result of the comparatively low V_T in trendy CMOS devices.Isub is calculated by exploitation the subsequent formula:

$$I_{SUB} = \frac{W}{L}\mu v_{th}^{2} C_{sth} e^{\frac{VGS-VT+\eta VDS}{\eta Vth}}(1-e^{-VDS/Vth})$$

where W and L denote the transistor breadth and length, μ denotes the carrier mobility, v_{th}=kT/q is that the thermal voltage at temperature T, C_{sth}=C_{dep}+ C_{it} it denotes the summation of the depletion region capacitance and therefore the interface entice capacitance each per unit space of the MOS gate , and is that the drain-induced barrier lowering (DIBL) constant. n is that the slope form factor and is calculated as:

$$n = 1+\frac{Csth}{Cox}$$

where Cox denotes the gate input capacitance per unit area of the MOS gate. When a long channel transistor with VDS larger than a few th is in the OFF state (VGS=0), we have:

$$I_{SUB} = \frac{W}{L}\mu v_{th}^{2} C_{sth} 10^{-V_T/S}$$

where S denotes the subthreshold swing parameter, that is outlined because the inverse of the slope of the log10(IDS) versus VGS characteristic and is equal to n th ln(10). S is equal to the subthreshold voltage decrease needed to extend ISUB by an element of 10. it's extremely fascinating to possess a subthreshold swing as tiny as possible since this is often the parameter that determines the number of voltage swing necessary to modify a MOSFET from OFF to ON state (typical values of S for bulk CMOS devices are 70-110 mV/decade; the theoretical lower bound is 60 mV/decade like n=1.) this is often particularly necessary for modern MOSFETs with offer voltages reaching sub-one volt region. to reduce S, the thinnest possible gate oxide (since it will increase Cox) and also the lowest possible doping concentration within the channel (since it decreases Cdep) should be used.

IV. Results & Discussion

Our propose work table for DGR algorithm with D0 is Delay at time 0 for random (monte carlo) analysis, Dub is Upper bound delay , Dlb is Lower bound delay , Dw is worse case delay, Db is best case delay, Lkw is worse case leakage power ,Lkb is best case leakage power.

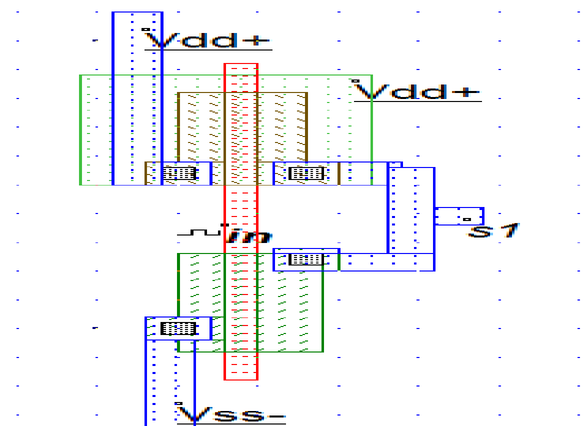

Fig.1. Layout Design of CMOS Inverter

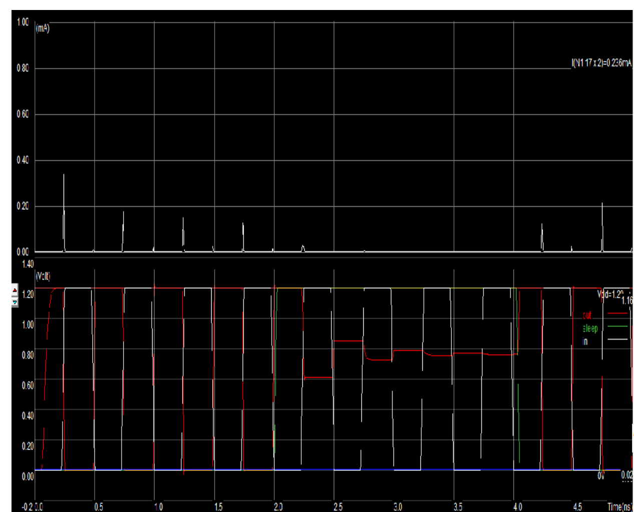

Fig.2. Leakage Current through N1 MOSFET of Inverter

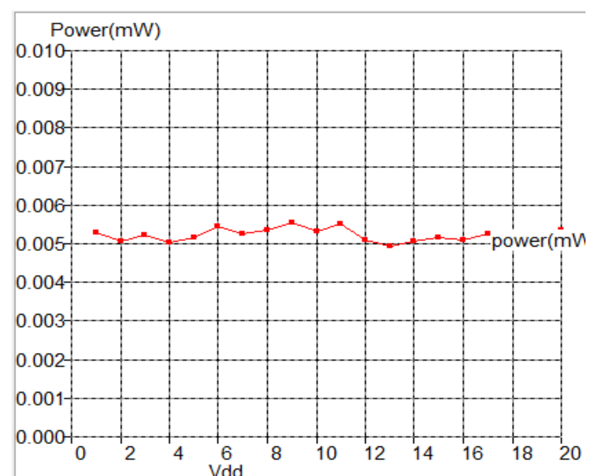

Fig.3. Power dissipation through Inverter.

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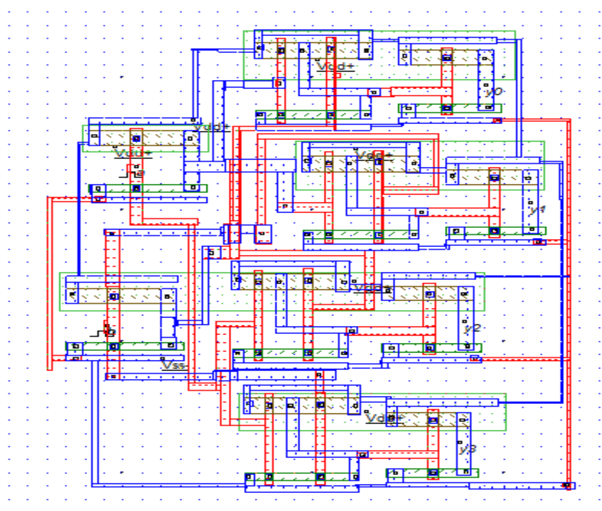

Fig.4 Layout Design of CMOS 4x1 Array Logic

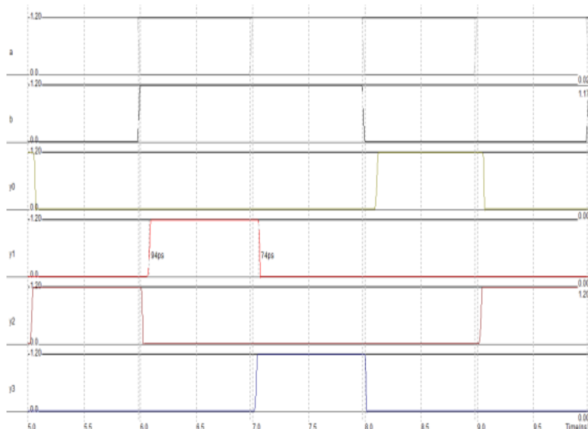

Fig.5. Timing Simulation of CMOS 4 x 1 Array Logic

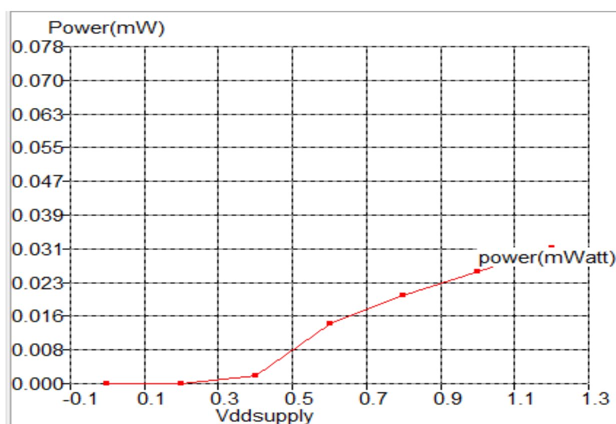

Fig.6. M Carlo Simulation For Power Dissipation of CMOS 4x1 Array Logic

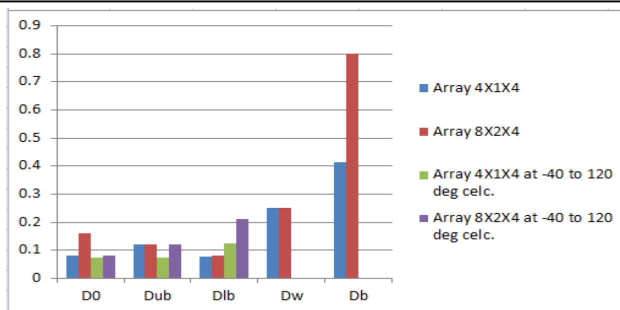

Fig.7 Delay analysis of 4X1 and 8X1 arrayLogic

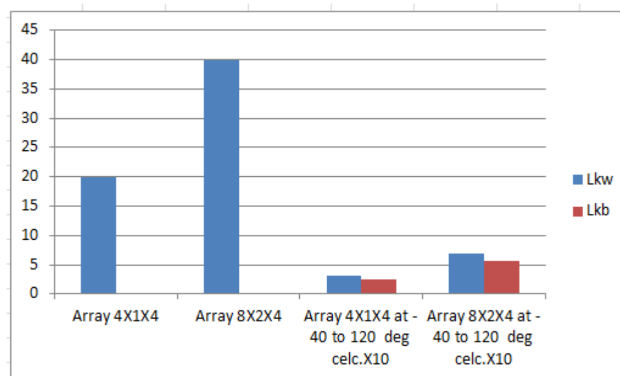

Fig.8 Leakage Power analysis of 4X1 and 8X1 array Logic

Fig.7 above represents the delay and leakage power analysis with D0 is Delay at time 0 for random (monte carlo) analysis, Dub is Upper bound delay , Dlb is Lower bound delay , Dw is worse case delay, Db is best case delay, Lkw is worse case leakage power ,Lkb is best case leakage power

This work reviewed numerous sources of leakage current in CMOS integrated circuits and represented variety of tested circuit improvement and software system techniques for controlling the OFF current of CMOS circuits in each standby and active modes of circuit operation. In means of enumerating a number of the planning challenges that lie ahead, we tend to mention the following:

- Need robust subthreshold leakage management techniques that don't adversely have an effect on the circuit performance and layout price. this can be particularly necessary in light-weight of each applied mathematics method parameter variations (VT,L,TOX) and environmental changes (temperature, offer voltage) and their impact on leakage currents
- Develop physical style tools that support multiple voltages on the chip, MTCMOS, and adaptive supply voltage and/or body biasing
- Consider power plane integrity in light-weight of sleep transistor insertions, accounting for each DC fall throughout the active mode, and ground bounce throughout the wakeup transition from sleep mode.
- Develop RT-level style flows and tools that enable early analysis and insertion of power gating structures and alternative leakage reduction mechanisms. Forcing a stack in each n- and p-networks of a gate can guarantee leakage reduction owing to stacking, freelance of the

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input logic level. stack forcing is applied to ways providing increase in delay owing to stacking doesn't violate temporal arrangement requirements. Gates which can force stack result freelance of its input vectors will mechanically go in leakage reduction mode once the intermediate node of the stack reaches the steady state voltage. this can boost standby and active leakage reduction.

V. Conclusion

We design the CMOS layout for inverter and 4X1 array logic in which we calculate the delay and leakage power analysis with D0 is Delay at time 0 for random (monte carlo) analysis, Dub is Upper bound delay , Dlb is Lower bound delay , Dw is worse case delay, Db is best case delay, Lkw is worse case leakage power ,Lkb is best case leakage power.

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