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A Non Linear Loop Filter Approach for Fast Locking Digital PLLVHDL AMS Simulation

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Abstract – The phase locked loop (PLL) is primary requirement for the synchronous communication system, because the clock synchronization is must for proper data receptions. In such systems the synchronization is performed by PLL. This paper presents a new design for the fast locking digital PLL which reduced the locking time greatly. The paper also presents the simulated results of the proposed DPLL in mixed signal environment by using VHDL-AMS. The VHDL-AMS is used here because of simplicity & its capability to perform the simulation of systems that contains both analog and digital components. Finally the simulation result shows that the proposed model performs well.

Keywords – Digital Phase Locked Loop, VHDL-AMS, Phase Frequency Detector.

1. INTRODUCTION

The basic work of a PLL is to track the frequency & to synchronize the local clock with given clock. Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to recover a signal from a noisy communication channel, generate stable frequencies at a multiple of an input frequency (frequency synthesis), or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz's. Inpresent scenario of digital systems a new type of PLL isused which are called Digital PLL and defined as type of PLL used to synchronize digital signals. While DPLLs input and outputs are typically all digital, they do have internal functions which are dependent on analog signals.
There are many digital PLL topologies have been already proposed by many authors using different enhancement in Adifferent part of the systems. In our approach we modified the charge pump section and made it non linear tracking fast changing signals quickly. The approach is inspired by the method proposed by the Dr. Mahmoud FawzyWagdy [1] et. al. they used some frequency comparators for quickly changing the response of loop filter we have taken the same topology for all other units as taken by them and given in [2]. The rest of the paper arranged as follows the second section presents a basic review on working of digital PLL with the components used then next section presents the proposed topology followed by simulation results and conclusion in next two sections.

2. DIGITAL PLL

Digital PLLs are a type of PLL used to synchronize digital signals. While DPLLs input and outputs are typically all digital, they do have internal functions which are dependent on analog signals. There are four basic components of a DPLL [3].

- Phase Detector
- Loop Filter
- Voltage Controlled Oscillator (VCO)
- Divider

The block diagram of the basic digital PLL is shown in Figure 1.

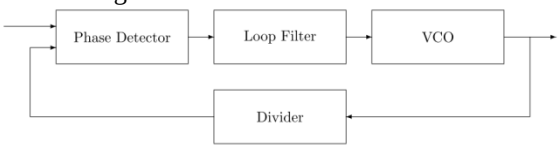

Fig.1. Block Diagram of Basic Digital PLL

Phase Detector: the work of this section is to compare the phase of the input clock with VCO clock and produce the output respectively generally two types of phase detectors are used, an XOR gate and a phase frequency detector (PFD), both have significantly different characteristics.
XOR Phase Detector **:** this is a two input XOR gate and it utilizes the property of XOR gate. Since the XOR produces the logic high whenever it detects the non similar inputs and that can be seen as the phase difference between two inputs. The behavior of XOR phase detector is defined below:

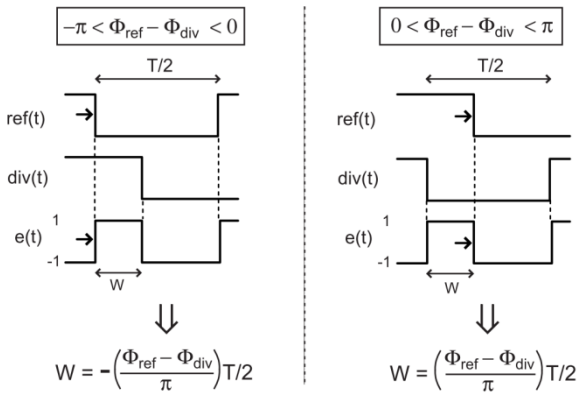

Fig.2. XOR Phase Detector Calculation

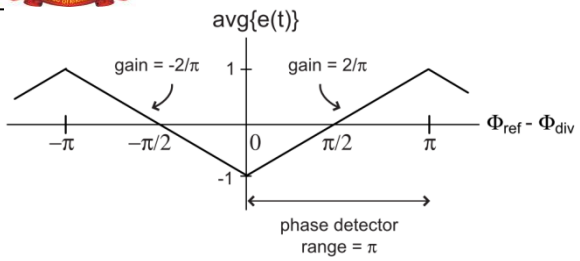

Fig.3. Output Average Value with Phase Error for XOR Phase Detector

The above figure shows that it having problem with direct detection of leading and lagging phases we need some additional system to do this particular task.

Phase Frequency Detector (PFD): The output of the PFD depends on both the phase and frequency of the inputs. This type of phase detector is also termed a sequential phase detector. It compares the leading edges of the ref(t) and div(t).

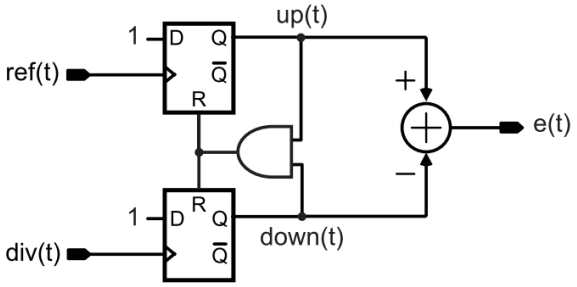

Fig.3. Circuit Diagram of Phase Frequency Detector (PFD)

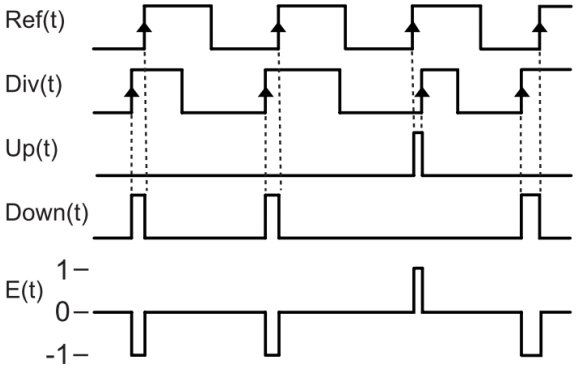

Fig.4. Waveforms shows the behavior of PFD

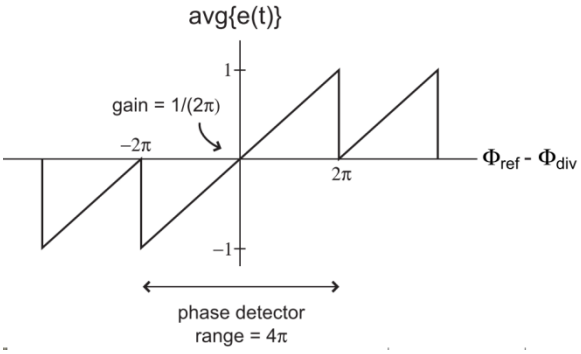

Fig.5. Average Value calculation for PFD

Loop Filter: The loop filter translates the error signals generated by the PD or PFD to some sort of analog voltage which is required to control the VCO. Generally it is implemented by analog low pass filters. It could be simple RC filter or an Active LPF.

Voltage Controlled Oscillator (VCO): Generate a Digital clock. The frequency of the clock generated is controlled by one or more voltage input. In the DPLL it is made to generate the square wave signals controlled by the input provided by loop filter.

Divider: The divider performs frequency division on the output signal to generate a signal which has the frequency of the input but the phase of the output. This component is not present on DPLLs which are designed to have an input frequency equal to the output frequency.

3. PROPOSED DIGITAL PLL

The proposed digital PLL is similar to basic digital PLL but it contains a non linear method to control the charge pump (the loop filter). The basic block diagram of the proposed PLL is given below

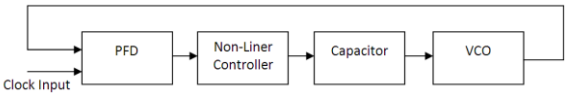

Fig.6. Block Diagram of Proposed digital PLL

The PFD and the VCO used in the proposed system is same as described in section 2. But the loop filter is modified as shown below

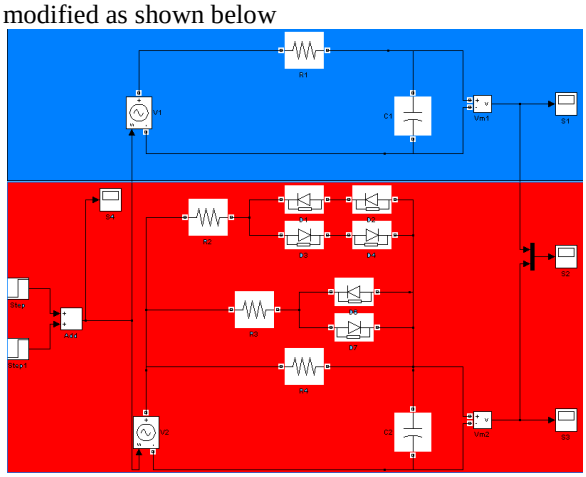

Fig.7. The Simulink Model of Standard (in Blue) and proposed (in Red) filter model

As shown in figure 7 the attached diodes changes the charging rate of capacitor after input rises to 0.7V and 1.4V hence at higher difference the charging rate increases quickly (like course tuning) and when difference fall to below 0.7V it slowly locks it. The explanation can be seen in figure 8 which shows the simulated results of tracking step changing input

voltage & it shows that the proposed method tracks very quickly.

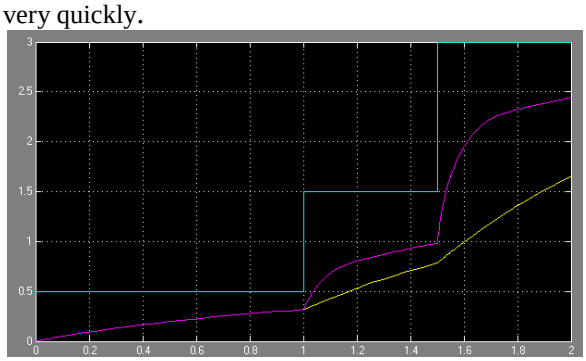

Fig.8. Simulation Results for step changing input (white) tracked by standard filter (green) and Proposed filter (blue)

Finally the results for the complete proposed PLL simulated in VHDL-AMS is shown below

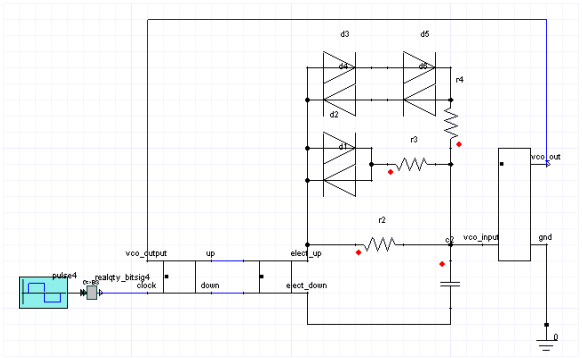

Fig.9. the simulated model of proposed digital PLL

Simulation Specifications:
Centre frequency = 2 GHz.
Change in frequency per volts for VCO = 300MHz.
Tracking Frequency = 2 GHz& 0.8 GHz.

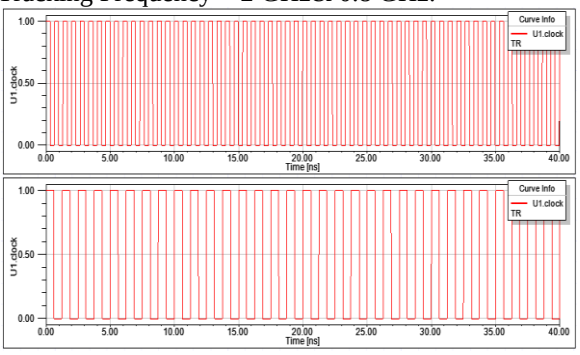

Fig.10. The clock input for tracking2 GHz (above) 0.8 GHz (below)

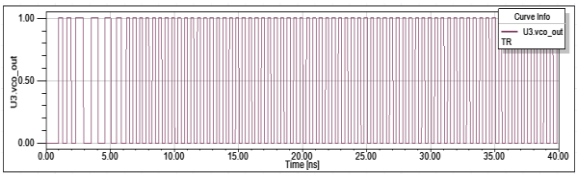

Fig.11. The clock input tracked by standard digital PLL shows a lot of variations and larger time to get locked

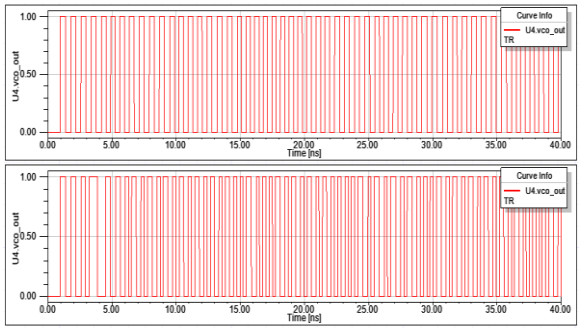

Fig.12. The clock input tracked by proposed digital PLL shows smooth tracking and quick locking

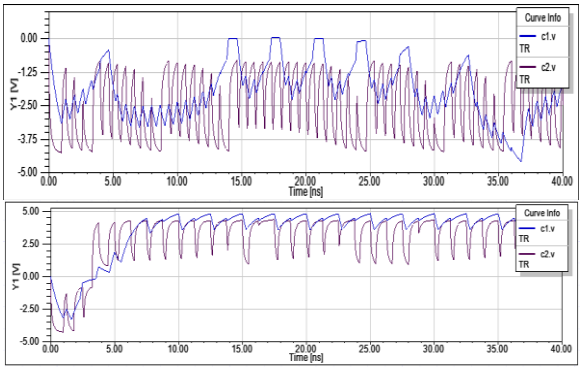

Fig.13. output of the loop filter for standard (in Blue) and proposed (in Red)

4. CONCLUSION

The simulation result shows that the proposed digital PLL tracks the variations very quickly and remains lock constantly it takes only approximately 3 ns for locking with 2 GHz and approximately 4 ns for locking with 0.8 GHz hence the proposed technique can be adopted for the quick locking digital PLL's, for the future prospects we can try to estimate the effects of varying the number of parallel diode circuit.DPLL's employ phase tracking which takes long time to lock, thus they become misfits for contemporary high-speed applications. Fast locking is therefore a necessity for clock/data recovery circuits, frequency-hopping spread-spectrum communications, cellular phones, etc.

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